

PATENT COOPERATION TREATY



(13)

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference WK04-043-PCT		FOR FURTHER ACTION See Form PCT/PEA/416	
International application No. PCT/JP2004/018432	International filing date (day/month/year) 03.12.2004	Priority date (day/month/year) 24.12.2003	
International Patent Classification (IPC) or national classification and IPC H01L29/739, H01L29/78, H01L29/10			
Applicant TOYOTA JIDOSHA KABUSHIKI KAISHA et al.			
<p>1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.</p> <p>2. This REPORT consists of a total of 6 sheets, including this cover sheet.</p> <p>3. This report is also accompanied by ANNEXES, comprising:</p> <p>a. <input checked="" type="checkbox"/> sent to the applicant and to the International Bureau a total of 4 sheets, as follows:</p> <p style="margin-left: 40px;"><input checked="" type="checkbox"/> sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).</p> <p style="margin-left: 40px;"><input type="checkbox"/> sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.</p> <p>b. <input type="checkbox"/> (sent to the International Bureau only) a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).</p>			
<p>4. This report contains indications relating to the following items:</p> <p><input checked="" type="checkbox"/> Box No. I Basis of the opinion</p> <p><input type="checkbox"/> Box No. II Priority</p> <p><input type="checkbox"/> Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability</p> <p><input checked="" type="checkbox"/> Box No. IV Lack of unity of invention</p> <p><input checked="" type="checkbox"/> Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement</p> <p><input type="checkbox"/> Box No. VI Certain documents cited</p> <p><input type="checkbox"/> Box No. VII Certain defects in the international application</p> <p><input type="checkbox"/> Box No. VIII Certain observations on the international application</p>			
Date of submission of the demand 06.10.2005		Date of completion of this report 22.03.2006	
Name and mailing address of the international preliminary examining authority:  European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016		Authorized Officer Baillet, B Telephone No. +31 70 340-3379 	

**INTERNATIONAL PRELIMINARY REPORT
ON PATENTABILITY**

International application No.
PCT/JP2004/018432

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.
- ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
- ☐ international search (under Rules 12.3 and 23.1(b))
 - ☐ publication of the international application (under Rule 12.4)
 - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)
2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages

1-33 as originally filed

Claims, Numbers

1-9 received on 06.10.2005 with letter of 03.10.2005

Drawings, Sheets

1/17-17/17 as originally filed

- ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing
3. ☐ The amendments have resulted in the cancellation of:
- ☐ the description, pages
 - ☐ the claims, Nos.
 - ☐ the drawings, sheets/figs
 - ☐ the sequence listing (*specify*):
 - ☐ any table(s) related to sequence listing (*specify*):
4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
- ☐ the description, pages
 - ☐ the claims, Nos.
 - ☐ the drawings, sheets/figs
 - ☐ the sequence listing (*specify*):
 - ☐ any table(s) related to sequence listing (*specify*):

* If item 4 applies, some or all of these sheets may be marked "superseded."

**INTERNATIONAL PRELIMINARY REPORT
ON PATENTABILITY**

International application No.
PCT/JP2004/018432

Box No. IV Lack of unity of invention

1. ☐ In response to the invitation to restrict or pay additional fees, the applicant has:
- ☐ restricted the claims.
 - ☐ paid additional fees.
 - ☐ paid additional fees under protest.
 - ☐ neither restricted nor paid additional fees.
2. ☒ This Authority found that the requirement of unity of invention is not complied with and chose, according to Rule 68.1, not to invite the applicant to restrict or pay additional fees.
3. This Authority considers that the requirement of unity of invention in accordance with Rules 13.1, 13.2 and 13.3 is
- ☐ complied with.
 - ☒ not complied with for the following reasons:
see separate sheet
4. Consequently, this report has been established in respect of the following parts of the international application:
- ☒ all parts.
 - ☐ the parts relating to claims Nos. .

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement
- | | | |
|-------------------------------|-------------|-----|
| Novelty (N) | Yes: Claims | 1-9 |
| | No: Claims | |
| Inventive step (IS) | Yes: Claims | 1-9 |
| | No: Claims | |
| Industrial applicability (IA) | Yes: Claims | 1-9 |
| | No: Claims | |

2. Citations and explanations (Rule 70.7):

see separate sheet

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**INTERNATIONAL PRELIMINARY
REPORT ON PATENTABILITY
(SEPARATE SHEET)**

International application No.

PCT/JP2004/018432

Reference is made to the following documents:

- D4: US-B1-6 518 629 (KUSHIDA TOMOYOSHI ET AL) 11 February 2003 (2003-02-11)
D6: PATENT ABSTRACTS OF JAPAN vol. 1997, no. 03, 31 March 1997 (1997-03-31) -& JP 08 316479 A (MITSUBISHI ELECTRIC CORP), 29 November 1996 (1996-11-29)

Re Item IV

Lack of unity of invention

1. This Authority considers that there are 3 inventions covered by the claims indicated as follows:

I: Claims 1, 2 and 9, as depending on claim 1, directed to an IGBT comprising an intermediate region of a first semiconductor type and a barrier region of a second conductivity type formed within the intermediate region.

II: Claims 3 and 9, as depending on claim 3, directed to an IGBT comprising an intermediate region of a first semiconductor type and a barrier region of the first semiconductor type formed within the intermediate region.

III: Claims 4-8 and 9, as depending on one of claims 4-8, directed to an IGBT comprising an intermediate region of the first conductivity type and a plurality of barrier regions formed within the intermediate region.

1.1 The reasons for which the inventions are not so linked as to form a single general inventive concept, as required by Rule 13.1 PCT, are as follows:

1.2 The common technical features between inventions I, II and III as disclosed above, are an IGBT comprising an intermediate region of a first conductivity type and a barrier region formed within the intermediate region. However, document D4 discloses (see D4, column 4, line 66 to column 5, line 13 and figure 7) an IGBT having a barrier layer formed in the intermediate region. Hence the common technical features between inventions I, II and III is not new and cannot be considered as a common inventive concept.

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

2. The document D6 is regarded as the closest prior art to the subject-matter of claim 1 and discloses (the references in parentheses applying to this document) an IGBT comprising an emitter electrode (45), a top region of the second conductivity type (45) connected to the emitter electrode, a deep region of the second conductivity type (42), an intermediate region of a first conductivity type (44) insulating the top region and the deep region, a collector region of the first conductivity type (41) connected to the deep region and being isolated from the intermediate region by the deep region, a collector electrode (52) connected to the collector region, a gate electrode (49) facing a portion of the intermediate region via an insulating layer (56), the intermediate region comprising a dense portion (91) directly connected to the emitter electrode.

2.1 The subject-matter of claim 1 differs from the content of D6 in that the IGBT of claim 1 comprises a barrier region comprising a semiconductor region of the second conductivity type formed within the intermediate region, this barrier region being in contact with the dense region and separated from the deep region by the main portion. The subject-matter of claim 1 is therefore new (Article 33(2) PCT).

2.2 The existence of the barrier region in contact with the dense portion, causes the accumulation of the minority carriers in the intermediate region, which reduces the on-voltage of the IGBT. This is neither disclosed nor suggested in the prior art, hence claim 1 is considered as involving an inventive step (Article 33(3) PCT).

2.3 Claims 2 and 9, when depending on claims 1 or 2, are dependant on claim 1 and as such also meets the requirements of the PCT with respect to novelty and inventive step.

3. Document D4 is regarded as being the closest prior art to the subject-matter of claims 3 and 4 and shows (the references in parentheses applying to this document, see in particular its figures 7 and 8) an IGBT comprising an emitter electrode (28), a top region of a second conductivity type (24) connected to the emitter electrode, a deep region of the second conductivity type (12), an intermediate region of a first conductivity type (18) connected to the emitter electrode and isolating the top region and the deep region, a collector region of the first conductivity type (10) connected to the deep region

and isolated from the intermediate region by the deep region, a collector electrode (30) connected to the collector region, a gate electrode (22) facing a portion of the intermediate region via an insulating layer (20), and a plurality of barrier regions (14) formed within the intermediate region.

3.1 The subject-matter of claim 3 differs from the content of D4, in that in claim 3 the barrier region has the first conductivity type and has a higher concentration in impurities than the intermediate region. The subject-matter of claim 3 is therefore new (Article 33(2) PCT).

3.2 The first conductivity type doping of the barrier region allows the discharge of the minority carriers via the barrier region, hence repressing the latch up effect, which could be caused by the flow of the minority carriers through the emitter. This is neither disclosed nor suggested by the prior art, hence claim 3 is considered as involving an inventive step (Article 33(3) PCT).

3.3 Claim 9, when depending on claim 3, also meets as such the requirements of the PCT with respect to novelty and inventive step.

3.4 The subject-matter of claim 4 differs from the content of D4, in that in claim 4 the plurality of barrier region within the intermediate region are distributed along a direction extending between the top region and the deep region. The subject-matter of claim 4 is therefore new (Article 33(2) PCT).

3.5 This characteristic allows the accumulation of minority carriers throughout the intermediate region, then reducing the on-voltage and is neither disclosed nor suggested by the prior art, hence claim 4 is considered as involving an inventive step (Article 33(3) PCT).

3.6 Claims 5-8 and claim 9, when depending on claim 4, depend on claim 4 and as such also meet the requirements of the PCT with respect to novelty and inventive step.

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AP3 Rec'd PCT/PTO 05 JUN 2006

Amendments under Article 34(2)b of PCT

CLAIMS

- 5 1. A semiconductor device of IGBT comprising:
an emitter electrode;
a top region of a second conductivity type connected to the emitter
electrode;
a deep region of the second conductivity type;
10 an intermediate region of a first conductivity type isolating the top
region and the deep region;
a collector region of the first conductivity type connected to the deep
region, the collector region being isolated from the intermediate region by the
deep region;
15 a collector electrode connected to the collector region;
a gate electrode facing a portion of the intermediate region via an
insulating layer, the portion of the intermediate region isolating the top region
and the deep region; and
a barrier region comprising a semiconductor region of the second
20 conductivity type formed within the intermediate region,
wherein the intermediate region comprises a dense portion directly
connected to the emitter electrode, and a main portion connected to the emitter
electrode via the dense portion,
wherein the barrier region is in contact with the dense portion, and is
25 separated from the deep region by the main portion.
2. A semiconductor device according to claim 1,
wherein the barrier region further comprises an insulator.
- 30 3. A semiconductor device of IGBT comprising:

an emitter electrode;

a top region of a second conductivity type connected to the emitter electrode;

a deep region of the second conductivity type;

5 an intermediate region of a first conductivity type connected to the emitter electrode, the intermediate region isolating the top region and the deep region;

a collector region of the first conductivity type connected to the deep region, the collector region being isolated from the intermediate region by the
10 deep region;

a collector electrode connected to the collector region;

a gate electrode facing a portion of the intermediate region via an insulating layer, the portion of the intermediate region isolating the top region and the deep region; and

15 a barrier region comprising a semiconductor region of the first conductivity type formed within the intermediate region;

wherein the barrier region has a higher concentration of impurities than the intermediate region, and the barrier region is formed along a boundary between the top region and the intermediate region, and is electrically connected
20 to the emitter electrode.

4. A semiconductor device of IGBT comprising:

an emitter electrode;

25 a top region of a second conductivity type connected to the emitter electrode;

a deep region of the second conductivity type;

an intermediate region of a first conductivity type connected to the emitter electrode, the intermediate region isolating the top region and the deep region;

a collector region of the first conductivity type connected to the deep region, the collector region being isolated from the intermediate region by the deep region;

a collector electrode connected to the collector region;

5 a gate electrode facing a portion of the intermediate region via an insulating layer, the portion of the intermediate region isolating the top region and the deep region; and

a plurality of barrier regions formed within the intermediate region;

10 wherein the barrier regions are distributed within the intermediate region along a direction extending between the top region and the deep region.

5. A semiconductor device according to claims 4,

15 wherein the intermediate region comprises a dense portion directly connected to the emitter electrode, and a main portion connected to the emitter electrode via the dense portion,

wherein at least one of the barrier regions is formed in the vicinity of a boundary between the dense portion and the main portion,

20 wherein at least the other of the barrier regions is the second conductivity type, is formed in the vicinity of a boundary between the main portion and the deep region, and is electrically disconnected from the emitter electrode and the deep region.

6. A semiconductor device according to claims 4,

25 wherein the intermediate region comprises a dense portion directly connected to the emitter electrode, and a main portion connected to the emitter electrode via the dense portion,

wherein at least one of the barrier regions is formed in the vicinity of a boundary between the dense portion and the main portion,

wherein at least the other of the barrier regions is the second conductivity type, is formed at a boundary between the main portion and the deep region, and has a higher concentration of impurities than the deep region.

5 7. A semiconductor device according to claims 5 or 6,
wherein at least a portion of the barrier regions are located on a path
along which carriers flow.

8. A semiconductor device according to claims 7,
10 wherein a plurality of pairs of barrier layer and intermediate layer is
stacked.

9. A semiconductor device according to any one of the preceding claims,
wherein the thickness of the top region is less than the thickness of the
15 barrier region.